REMARKS

Claims 1-3, 5, and 7-30 are pending in this application. Claims 4 and 6 have been canceled without prejudice. Claims 3 and 7-29 have been withdrawn from consideration, as drawn to a non-elected invention.

Claims 1 and 2 have been amended to more clearly set forth the present invention. Claim 30 has been newly added to further define the present invention. Support for claims 1 and 2 as amended, and for new claim 30, appears throughout the specification and claims as originally filed. No new matter has been added.

The specification has been amended to correct minor errors. Specifically, page 7, line 24, has been amended to correctly recite "on the" in place of "ontha". No new matter has been added.

In view of the amendments to the claims, new claim 30, and the remarks set forth below, further and favorable consideration is respectfully requested.

1. ***At page 2 of the Office Action, the Examiner requires a new title, which is indicative of the claimed invention.***

Responsive to the Examiner's requirement, the title has been amended to recite:

A THIN-FILM CIRCUIT SUBSTRATE

Accordingly, the Examiner is respectfully requested to withdraw this objection.

2. ***At page 3 of the Office Action, the Examiner objects to the disclosure because the Japanese priority application is incorrectly identified on page 21 of the specification.***

Responsive to the Examiner's request, the specification has been amended on page 21, lines 8 and 9, to recite the proper Japanese priority application number, *i.e.* JPA 2001-262359, filed on August 30, 2001. Accordingly, the Examiner is respectfully requested to withdraw this rejection.

3. ***At page 3 of the Office Action, the Examiner has objected to the drawings because Figs. 1 and 2 should be labeled "prior art."***

Responsive to the Examiner's objection, submitted herewith please find corrected Figs. 1 and 2, properly labeled "prior art." Accordingly, the Examiner is respectfully requested to withdraw this objection.

4. ***At pages 3 and 4 of the Office Action, claims 1, 2 and 4-6 have been rejected under 35 USC §102(e) as being anticipated by Chu et al. (USP Application Publication No. 2002/0109231 A1).***

The Examiner states that Figs. 3 and 4C illustrate the invention, as presently claimed in claims 1, 2 and 4-6.

Chu is directed to a capacitor formed on a conductive plug of a semiconductor substrate that includes a composite storage node. Fig. 3 discloses a semiconductor substrate 20 including polysilicon plugs 24, and a first insulating layer 22 deposited on the substrate.

Anticipation under 35 USC §102 requires that a single prior art reference teach each and every element of the claimed invention.

In view of the following this rejection is believed to be overcome.

Present claim 1 has been amended to require that a conductive material is filled in the through holes, and to require that the thin-film circuit layer formed on the first insulator layer, has a flat face which contacts the first insulator layer and the electrically conductive material in the through holes.

The present invention relates to a via-formation substrate used for an interposer provided between external substrates or alternatively provided on an external substrate in the form of a three-dimensional stack.

Thus, in the thin film circuit substrate of the present invention the first insulator layer and the thin film circuit layer are formed on one surface (first principal plane) thereof, and the through holes extend continuously from the opposite surface (second principal plate) thereof. Each of the through holes is formed of the electrically conductive material filling the through hole and the second insulator layer covering the side wall face of the through hole. The through holes include a main section having a first diameter and a tapered section having a second diameter larger than the first diameter near the first principal plane. The film circuit layer of the thin film circuit substrate has a flat face in which the first insulator layer and the electrically conductive material (inside the through hole) make contact.

Because such a construction enables formation of the thin-film circuit layer before the step of forming the via plug (electrically conductive material), the present invention is advantageous because it eliminates the previously required mirror polishing process performed

after the step of forming the via plug (conductive material). Please see Fig. 4 of the present invention.

Chu et al., on the other hand, describe a storage node for storing information in a capacitor.

Chu et al. provide a circuit similar to the one shown in Fig. 1 thereof on a Si substrate 20 as schematically represented in Fig. 3. Specifically, Chu et al. disclose only storage nodes of high-K capacitors on the substrate 20, not the presently rquired thin-film circuit.

In addition, Chu et al. include a MOS circuit (integrated circuit) formed in the upper part of the substrate 20 as shown in Fig. 3 thereof. However, the insulator 22 is not formed on the bulk silicon substrate as presently rquired, but on the interlayer insulation film including a bit line 10 (see Fig. 1 of Chu et al.) provided on the silicon bulk substrate so as to cover the MOS devices. Thus, the Si substrate 20 of Chu et al., is not a bulk silicon substrate, contrary to the present invention.

Chu et al. do not teach a through hole including "a main section substantially having a first diameter and extending from the second principal plane, and a tapered section having a second diameter that is larger than the first diameter near the first principal plane" of the semiconductor substrate, as presently required. In Chu et al., the through hole has a uniform diameter inside the silicon substrate defined by the first and second principal planes.

Further, Chu et al. do not teach "the second insulator layer that covers a side wall face of the through holes", as required by the present claims.

Chu does not teach a conductive material filled in the through holes, and does not teach a thin-film circuit layer formed on a first insulator layer, having a flat face which contacts the first insulator layer and the electrically conductive material in the through holes, as presently required.

In view of the amendments to the claims and remarks set forth above, it is submitted that Chu does not teach each and every element of the claimed invention, as required for anticipation, under 35 USC §102. Accordingly, the Examiner is respectfully requested to withdraw this rejection.

5. ***At page 5 of the Office Action, claims 1, 2, 4 and 6, have been rejected under 35 §102(b) as being anticipated by Northrop et al. (USP 5,882,496).***

The Examiner contends that Northrop meets the limitations of the presently claimed invention because Northrop discloses a substrate including a first insulation layer 14, a second insulator layer 16, a tapered through hole 15 and a second insulator layer 16 that covers a side wall face of the through hole and a thin-film circuit.

Northrup does not teach a thin-film circuit, as required by amended claim 1. For example, Fig. 1 of Northrop does not disclose any structure corresponding to the thin-film circuit of the present invention. The layer 14 of Northrop, provided on the silicon substrate 10, is a silicon nitride layer and does not form a thin-film circuit. Further, another silicon nitride layer 16 is provided on the other side of the depression in Northrop.

Thus, Northrop does not teach a through hole, as presently required.

In addition, the through hole of the present invention performs the function of transmitting a signal from the thin-film circuit formed on the first plane to the second plane, and

thus, the through hole must include an insulation film (second insulation film of the present invention) covering the sidewall surface of the through hole in order to electrically insulate the conductive plug formed in the through hole.

Northrop does not teach an insulation film covering the sidewall surface of the porous silicon layer 12 or the diffusion region 13. Thus, the structure of Northrop as shown in Figs. 1-3 cannot perform the function of the through hole of the present invention.

In view of the amendments to the claims and remarks set forth above, it is submitted that Northrop does not teach each and every element of the claimed invention, as required for anticipation, under 35 USC §102. Accordingly, the Examiner is respectfully requested to withdraw this rejection.

In view of the aforementioned amendments and accompanying remarks, claims 1-2, 5-6 and 30, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Petition for Extension of Time

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